**ABSTRACT**

The SoC (System on Chip) uses AMBA (Advanced Microcontroller Bus Architecture) as an onchip bus. APB (Advanced Peripheral Bus) is one of the components of the AMBA bus architecture. APB is low bandwidth and low performance bus used to connect the peripherals like UART, Keypad, Timer and other peripheral devices to the bus architecture. This paper introduces the AMBA APB bus architecture design. The design is created using the verilog HDL and is tested by a verilog testbench. This design is verified using UVM (Universal Verification Methodology).

In this project, I have developed synthesizable design of APB UVM testbench for the functional verification of the same in system verilog HDL. I have also written shell script for testing the required feature only at a time. The software tools that I have used are GVim (Text Editor), Questa Sim (Verilog Compiler and Simulator).

**TABLE OF CONTENTS**

|  |  |  |
| --- | --- | --- |
| **CHAPTER NO.** | **TITLE** | **PAGE NO.** |
|  | **ACKNOWLEDGEMENT** |  |
|  | **ABSTRACT** |  |
|  | **LIST OF FIGIRES** |  |
|  | **LIST OF ABBREVIATIONS** |  |
| **1** | **INTRODUCTION** | **1** |
| 1.1 | ARM | **1** |
| 1.2 | ARM AMBA | **2** |
| 1.3 | APB | **2** |
| 1.4 | AMBA ARCHITECTURE | **3** |
| 1.5 | SIGNAL DESCRIPTION | **4** |
| **2** | **LITERATURE SURVEY** | **6** |
| **3** | **DESIGN** | **8** |
| 3.1 | APB INTERFACE WITH SLAVES | **8** |
| 3.2 | TRANSFERS | **9** |
| 3.3 | OPERATING STATES | **12** |
| 3.4 | SYSTEM VERILOG | **13** |
| **4** | **VERIFICATION** | **16** |
| 4.1 | UVM | **16** |
| 4.2 | UVM PHASES | **19** |
| 4.3 | UVM CODING | **21** |
| **5** | **IMPLEMENTATION** | **28** |
| 5.1 | SOFTWARE TOOLS USED | **28** |
| 5.2 | APB DESIGN CODE | **28** |
| 5.3 | MASTER CODE | **30** |
| 5.4 | SLAVE-1 CODE | **38** |
| 5.5 | SLAVE-2 CODE | **40** |
| **6** | **RESULTS** | **42** |
| 6.1 | WRITE OPERATION | **42** |
| 6.2 | READ OPERATION | **43** |
|  | **CONCLUSION** | **44** |
|  | **REFERENCES** | **45** |

**LIST OF FIGURES**

|  |  |  |
| --- | --- | --- |
| **FIGURE NO.** | **TITLE** | **PAGE NO.** |
| 1.1 | AMBA SPECIFICATIONS | 2 |
| 1.2 | AMBA BUS ARCHITECTURE | 4 |
| 3.1 | APB INTERFACE WITH SLAVES | 8 |
| 3.2 | WRITE TRANSFER WITH NO WAIT STATES | 9 |
| 3.3 | WRITE TRANSFER WITH WAIT STATES | 10 |
| 3.4 | READ TRANSFER WITH NO WAIT STATES | 11 |
| 3.6 | STATE DIAGRAM | 12 |
| 3.7 | EVOLUTION OF SYSTEM VERILOG | 14 |
| 3.8 | SYSTEMVERILOG COMPONENTS | 15 |
| 4.1 | POSITION OF RTL VERIFICATION IN THE VLSI DESIGN FLOW | 16 |
| 4.2 | UVM ARCHITECTURE | 17 |
| 4.3 | UVM VERIFICATION COMPONENTS | 18 |
| 6.1 | SIMULATION RESULT | 42 |
| 6.2 | WRITE OPERATION | 42 |
| 6.3 | READ OPERATION | 43 |

**LIST OF ABBREVIATIONS**

|  |  |
| --- | --- |
| ARM | Advanced RISC Machine |
| RISC | Reduced Instruction Set Computing |
| SoC | System-on-Chip |
| SoM | Systems-on-Modules |
| CISC | Complex Instruction Set Computing |
| AMBA | Advanced Microcontroller Bus Architecture |
| APB | Advanced Peripheral Bus |
| AHB | Advanced High-performance Bus |
| ASB | Advanced System Bus |
| UVM | Universal Verification Methodology |
| DUT | Design Under Test |